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Title: AMBA 3 APB Protocol Specification Author: ARM Limite Feb 5th, 2024

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AXI Reference Guide - Xilinx

AXI Reference Guide Www.xilinx.com 5 UG761 (v13.1) March 7, 2011 Chapter 1 Introducing AXI For Xilinx System Development Introduction Xilinx® Has Adopted The Advanced EXtensible Interface (AXI) Protocol For Intellectual Property (IP) Cores Beginning With The Sparta Feb 2th, 2024

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For More Information On The Spartan-6 Devices, See The Spartan-6 Family Overview [Ref 5]. 5. For The Supported Versions Of The Tools, See The ISE Design ... Contains The State Machine For The IIC Bus Operations. Dynamic Master: ... A 100 MHz Clock Coupled With An C_SCL_ May 2th, 2024

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AXI Bridge For PCI Express V2.5 Www.xilinx.com 8 PG055 November 19, 2014 Chapter 2 Product Specification Figure 2-1 Shows The Architecture Of The AXI Bridge For PCI Express® Core. The Register Block Contains Registers Used In The AXI Bridge For PCI Express Core For Dynamically Mapping The AXI4 Memory Mapped (MM) Address Range Provided Using The Jan 5th, 2024

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LogiCORE IP AXI Video Direct Memory Access V6

"Video IP: AXI Feature Adoption" Section Of The AXI Reference Guide (UG761). AXI4 Data Width The AXI VDMA Core Supports The Primary AXI4 Data Bus Width Of 32, 64, 128, 256, 512, And 1024 Bits. AXI4-Stream Data Width The AXI VDMA Core Supports The Primary AXI4-S Tre Apr 3th, 2024

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