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Chair 2S No Arm 3S No Arm 3 3S 1arm(LHF) seater Settee 2 Seater Settee 2.5 Seater

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1 Arm J1:1 - A518 (W) T Arm J1:2 - A518 (E) - Straight

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0 5 10 15 20 25 30 35 40 1 2 4 MIPS Number Of Cores (Instruction Set Simulators) Avg. ISS MIPS Acc. System MIPS 3 VP Simulation Performance N Example: UC/MC VP Performance (MIPS)-Target SW: COREMARK/Linux-Test Single/dual/quad Core Systems-In-house Instruction Set Simulator (ISS)-OSCI/Accellera1SystemC KernelReduced Simulation Feb 5th. 2024

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