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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [Jan 10th, 2024

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A Complete ASIC Design Of The Cryptosystem Is Presented. The Designed ASIC Was Found To Be More E Cient (parameterized As Throughput/area) Than All Reported Works. The Thesis Also Deals With The Design Of A Special Purpose Hardware For Cryptanalysis Of AES Rijndael. { Title Of PhD Thesis: Apr 16th, 2024

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